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MODULE DESCRIPTOR

Module Title

Electronics 3

Reference	EN3512	Version	8
Created	April 2022	SCQF Level	SCQF 9
Approved	July 2009	SCQF Points	15
Amended	May 2022	ECTS Points	7.5

Aims of Module

To provide students with the ability to analyse and synthesise analogue and digital circuits and systems.

Learning Outcomes for Module

On completion of this module, students are expected to be able to:

1	Design analogue circuits and systems.
2	Create and evaluate analogue circuits and systems.
3	Analyse and design digital RTL systems.
4	Design and implement digital systems using programmable logic.

Indicative Module Content

Differential and instrument amplifier design, analysis and simulation. Design and evaluation of voltage regulator circuits and analysis of its heat dissipation. Active filter design and study of their application in biomedical signal acquisition. Analogue signal acquisition and processing in a Virtual Instrument (VI) environment; basic VI structures for signal capture, analysis and recording. Sequential digital design and implementation using Algorithmic State Machines (ASM); High-level state machines and Register Transfer Level(RTL). The use of programmable logic and high-level description languages in digital system design and implementation.

Module Delivery

Full-time students: This module is delivered by a combination of lectures and tutorials. It will be supported by practical examples and activities including computer based laboratory exercises. Part-time students: This module is delivered by a combination of lectures and tutorials online. It will be supported by drop-in evening sessions and labs on campus. Assessments will primarily be online although exams will be held on campus with the full-time cohorts.

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Indicative Student Workload	Full Time	Part Time
Contact Hours	45	45
Non-Contact Hours	105	105
Placement/Work-Based Learning Experience [Notional] Hours	N/A	N/A
TOTAL	150	150
Actual Placement hours for professional, statutory or regulatory body		

ASSESSMENT PLAN

If a major/minor model is used and box is ticked, % weightings below are indicative only.

Component 1

Type:	Coursework	Weighting:	30%	Outcomes Assessed:	2, 4
Description:	Design investigation.				

Component 2

Type:	Examination	Weighting:	70%	Outcomes Assessed:	1, 3
Description:	Closed book examination.				

MODULE PERFORMANCE DESCRIPTOR

Explanatory Text

The module has 2 components and to gain an overall pass a minimum D grade must be achieved in each component. The component weighting is as follows: C1 is worth 30% and C2 is worth 70%.

Examination:

	Coursework: A	B	C	D	E	F	NS
A	A	A	B	B	E	E	
B	B	B	B	C	E	E	
C	B	C	C	C	E	E	
D	C	C	D	D	E	E	
E	E	E	E	E	E	F	
F	F	F	F	F	F	F	

NS	Non-submission of work by published deadline or non-attendance for examination

Module Requirements

Prerequisites for Module	Electronics 2 (EN2510) or the equivalent.
Corequisites for module	None.
Precluded Modules	None.

ADDITIONAL NOTES

An Indicative Bibliography will normally reference the latest edition of a text. In some cases, older editions are equally useful for students and therefore, those are the editions that may be stocked.

INDICATIVE BIBLIOGRAPHY

1	BOTROS, N., 2005. HDL Programming Fundamentals: VHDL and Verilog. Rockland, MA: Charles River Media, Inc.
2	FRANCO, S., 2014. Design with Operational Amplifiers and Analog Integrated Circuits. 4th ed. New York, NY: McGraw-Hill.
3	ROTH, C. H., 2013. Fundamentals of Logic Design. 7th ed. Nashville, TN: Thomson/Nelson.
4	SEDRA, A.S. and SMITH, K.C., 2014. Microelectronic Circuits. 7th ed. New York, NY: Oxford University Press.